A GENERAL-PURPOSE CIRCUIT MODEL OF INTERDIGITAL CAPACITOR FOR ACCURATE DESIGN OF LOW-LOSS MICROSTRIP CIRCUIT[#]

Lei ZHU and Ke WU

POLY-GRAMES Research Center
Departement de Génie Electrique et de Génie Informatique
École Polytechnique de Montréal, C.P. 6079, Succ. Centre Ville
Montréal, Québec, Canada H3C 3A7

ABSTRACT

A general-purpose CAD-oriented circuit model is presented for accurately modeling interdigital capacitor (IDC) in optimized design of low-loss IDC-related microstrip circuits. This equivalent model is formulated as an admittance-based π-network through the use of a so-called "Short-Open Calibration (SOC)" technique for extracting precisely circuit parameters from a fullwave method of moments (MoM). A J-inverter based topology is further developed for explicit characterization of IDC-related coupling characteristics that accounts for frequency dispersion and fringing effect. Extracted model parameters are given for two types of IDC structure and the model accuracy is well validated by our experiments for an IDC-related quasi-lumped bandpass filter.

I. INTRODUCTION

Microstrip InterDigital Capacitor (IDC) has been widely used as a lumped element in high-frequency integrated and high-speed digital circuits [1-4]. In the very beginning, various 2-D static model-based analytical or numerical algorithms were usually applied for deriving its CAD model. Unfortunately, these CAD models had to ignore usually the fringing field effects of multiple finger ends [1, 2] or could approximately account for a partial amount of these effects such as the end capacitance [3]. This is mainly because these 2-D models were formulated from the modeling of a uniform coplanar strip structure, and it is very difficult for them to accommodate physical effects of the finger end discontinuity.

Very recently, a CAD lumped LC-network model [4] has been proposed and it was derived from a partial element description (PED) in a 3-D MoM. Nevertheless, this CAD model is valid only for a frequency range where the total IDC size is much small as compared to the operating wavelength. Since the strip width around the finger section is electrically much narrow in this case, parasitic effects such as conductance loss and strip thickness become too significant to be ignored [2].

In this work, an accurate CAD circuit model for a generalized IDC structure is formulated through the use of a so-called "Short-Open Calibration (SOC)" technique [6-7]. This model is self-contained in a hybrid-mode MoM algorithm [5]. This circuit model is at first defined as a general-purpose admittance π-network along two feed lines of IDC in question. Without resort to any hypothetical conditions in our technique, the developed model can account for all possible physical effects including frequency dispersion and fringing field effects for an IDC structure in a very broad frequency bandwidth as long as the accuracy of the MoM algorithm is concerned.

Considering the fact that our interests in the use of IDC structure are in the design of low-loss microstrip circuits which requires generally strong coupling elements, this admittance π-network circuit model is further transformed into a J-inverter topology that allows to have an explicit representation of the IDC coupling characteristics. In our following examples, calculated parameters including J-inverter susceptance and electrical length of the two connecting equivalent lines are given and the model accuracy is validated by our experiments for an IDC-related quasi-lumped bandpass filter.

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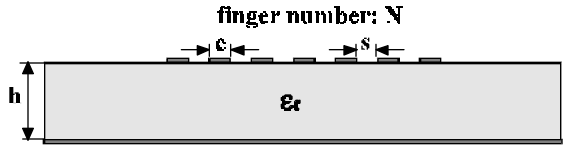
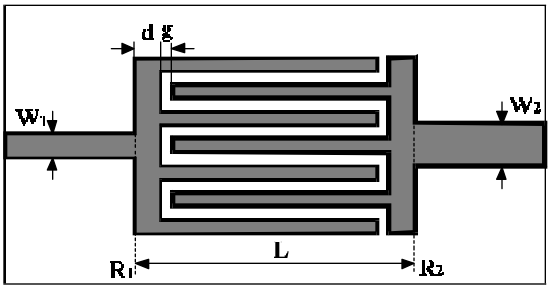
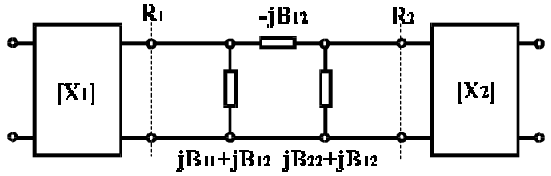
II. GENERAL-PURPOSE CIRCUIT MODEL



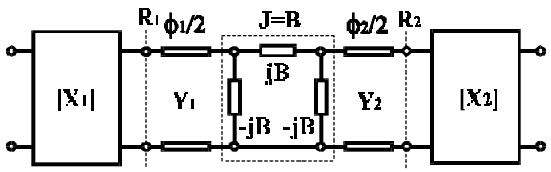
(a) cross-sectional view



(b) top view of layout



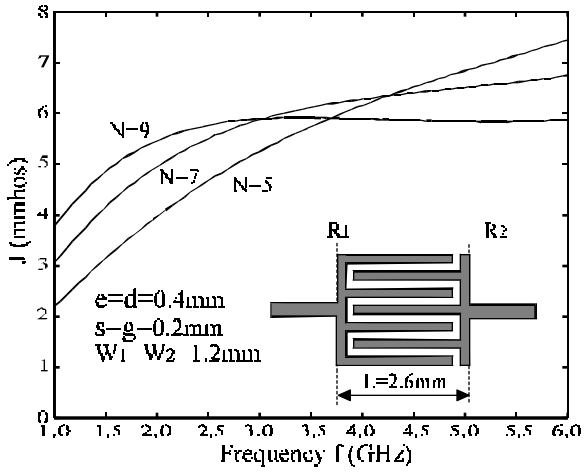
(c) admittance π-network



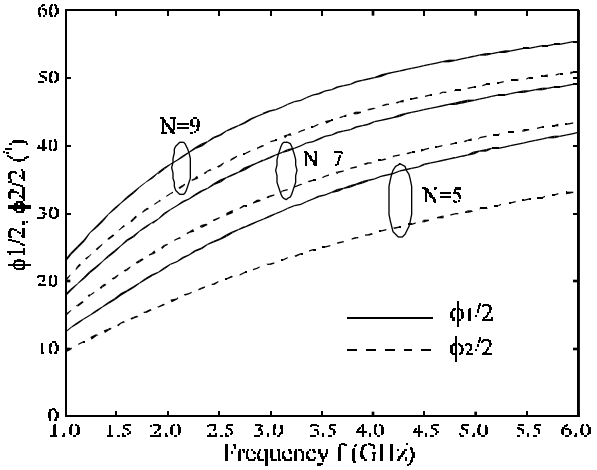
(d) J-inverter network

Fig.1 Physical description and its CAD-oriented circuit model of an IDC structure

Fig. 1(a) and (b) depict the cross-sectional view and geometrical sketch of an IDC structure that may be found in integrated M(H)MICs and digital ICs. In this IDC structure, the interdigital multiple fingers are externally attached with two lines serving the input and output for the IDC. To satisfy a general-purpose design requirement, the two lines are generally considered to be different in strip width. Fig. 1(c) describes its equivalent admittance π-network topology, attached with the two so-called error terms, namely, $[X_1]$ and $[X_2]$, that stand for parasitic approximate effects brought by the port discontinuity in a deterministic MoM algorithm [5]. Through characterization via the two standard calibration elements (short and open) implemented in this MoM algorithm and removal of these two error terms out of pre-calculated circuit parameters [6-7], this admittance based topology can be accurately de-embedded (extracted) at the specific locations, namely, R_1 and R_2. It can be represented as a susceptance π–network if the lossless case is considered.



(a) J-inverter susceptance



(b) equivalent electrical line length

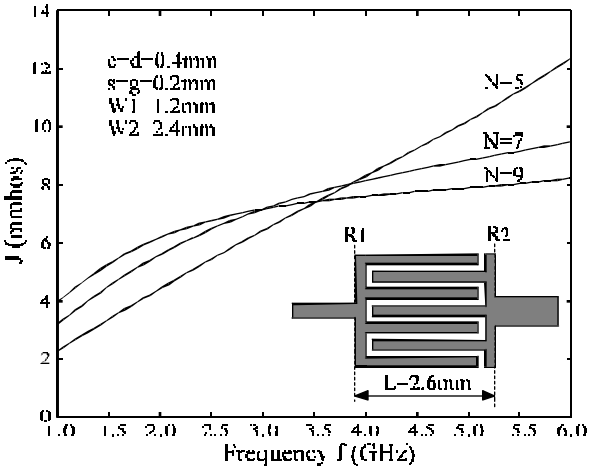
Fig.2 J-inverter network parameters for an IDC attached with two 50Ω lines: N=5,7,9

Judging from the design issue in connection with the IDC-related circuits, the obtained π–network is subsequently transformed into its corresponding J-inverter network with a susceptance and its two attached equivalent electrical lines as indicated in Fig. 1(d). This alternative representation of IDC circuit topology is rather useful for design and synthesis. The J-inverter susceptance is directly related to the coupling characteristics (strength) while the equivalence of two attached electrical

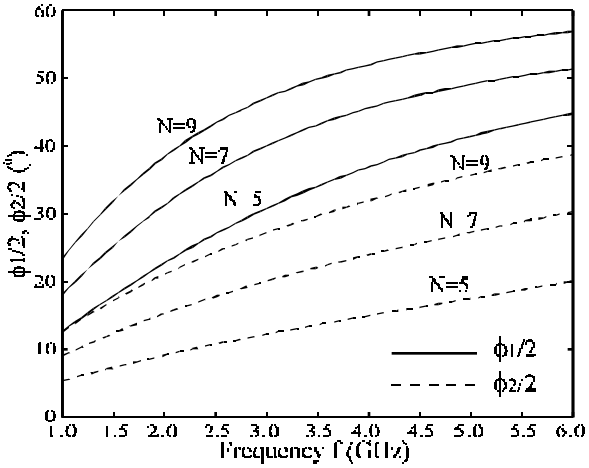
lines presents frequency-dependent fringing field effects and finger end discontinuities. The equivalence between the two network topologies allows to set up a general-purpose equation [7] that relates the J-inverter parameters to the $\pi-$network susceptance parameters.

Fig. 2 presents extracted frequency-dependent J-inverter susceptance and two equivalent electrical line lengths of an IDC structure for three different cases related to the finger number: N = 5, 7, 9. In this example, two identical 50 Ω lines are used to connect the IDC. It is observed in Fig. 2(a) that the J-inverter susceptance increases rapidly with N for frequency lower than 2.0 GHz, presenting actually lumped element characteristics of the limiting case for which the total IDC size is electrically smaller than the operating wavelength, as justified in [3-4]. However, the J-inverter susceptance tends to be gradually saturated for all of the three cases as the frequency increases. In particular, it seems to go downward at f = 2.5 GHz for N = 9. Beyond f = 4.0 GHz, the low-frequency lumped element behavior disappear completely, indicating the conventional approximate model is no longer valid in this case. It is attributed to high-frequency distributed inductive/capacitive fringing field effects at the finger end discontinuity. Parallely, the two electrical lengths, $\phi_1/2$ and $\phi_2/2$ are found to increase significantly with frequency, and they become large with the finger number N.

Fig. 3 shows J-inverter network parameters extracted for an IDC structure attached with two different lines with 50 Ω and 34 Ω, for N = 5, 7, 9. It is found that a similar behavior is applied for this case study with reference to Fig.2. Interestingly, the J-inverter susceptance seems to be enlarged to a certain extent as opposed to that shown in Fig. 2. This can be physically interpreted that the interface-related discontinuity effects between the finger section and external lines at the right side of IDC are reduced as the line width W_2 is widened toward the total width of finger section. By a similar explanation, the electrical length $\phi_2/2$ is found to be shortened with roughly 6^0 to 14^0 in the frequency range of interest. The electrical length $\phi_1/2$, however, appears approximately to be identical as compared to Fig. 2(b). In the following, these extracted model will be applied to the design and optimization of an IDC-related bandpass filter with a simple line resonator concept.



(a) J-inverter susceptance



(b) equivalent electrical line length

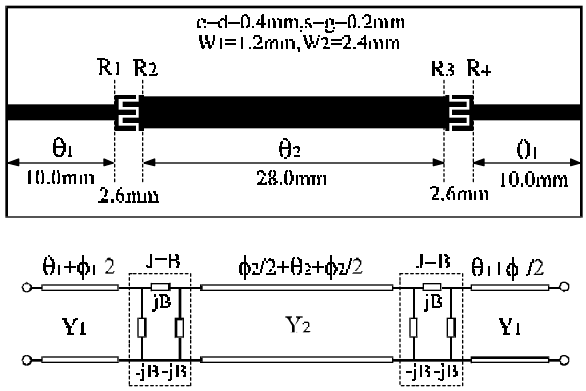
Fig.3 J-inverter network parameters for an IDC attached with 50Ω and 34 Ω lines: N=5,7,9

III. A DESIGN EXAMPLE

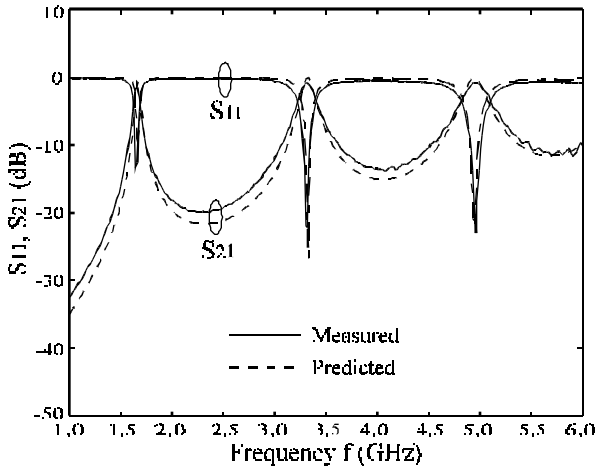
As described in Fig. 4(a), a bandpass filter layout is designed and synthesized by the proposed general-purpose J-inverter model for two asymmetrical IDCs that are interconnected by a line resonator. The input and output lines (50 Ω) are different from the line width of the resonator and the finger number N = 5 for the IDCs whose dimensions and topology are detailed in Fig. 3. The frequency response and other electrical characteristics of the filter can be easily derived from the complete model as indicated by the CAD-oriented model, as in Fig.4(a).

In this distributed model, the total electrical length (θ) related to the line resonator consists of two

parts, namely, the uniform section of the line (θ_2) and the two identical equivalent line lengths $\phi_2/2$, contributed by the two IDC models. Therefore, $\theta = \phi_2/2 + \theta_2 + \phi_2/2$, indicating that the resonant frequency of the line resonator should be strongly affected by the equivalent electrical length of the two IDC models. Since, in this model, the J-inverter susceptance indicates the coupling strength between the external lines and the line resonator, an appropriate insertion loss and bandwidth can be accurately predicted with the proposed model.



(a) design layout and its CAD-oriented model



(b) frequency response

Fig.4 CAD-oriented model and its predicted results compared to measured results for an IDC-related microstrip bandpass filter

The frequency response of calculated and measured scattering parameters of the filter is plotted together in Fig. 4(b), showing an excellent agreement in such a large frequency range (1.0 - 6.0 GHz).It is shown judging from the insertion loss S_{21} that the filtering bandwidth becomes broader with the order of three resonant frequencies. This is essentially due to the coupling enhancement via frequency in connection with the J-inverter susceptance behavior in the case of N = 5, as shown in Fig. 4(a).

IV. CONCLUSIONS

In this work, a general-purpose CAD-oriented circuit model is proposed for use in an accurate J-inverter network representation of IDC structure. This model is derived from a numerical "short-open calibration (SOC)" technique and it allows to accommodate frequency dispersion and other parasitic effects. It is shown that this model is very useful for accurate high-frequency design and synthesis related to the IDC topology. Our predicted electrical performance for an IDC-related bandpass filter is well compared with the measured results, showing the usefulness and accuracy of the proposed CAD and optimization strategy.

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